

3. Projects

Typical projects for this course include counters, shift-registers, flip-flops, multipliers, dividers and analog circuits such as an OTA (operational transconductance amplifier).

The digital circuits are suitable for both standard-height and bit-slice formats so the same schematic and pre-layout simulation can be used for both. However, the standard-height format must be of fixed height and its input and outputs aligned with a grid so that the cell can be automatically overlapped with its neighbors, as shown in Figure 2. The requirements for bit-slice cells is less restrictive but inputs and outputs are aligned horizontally while power and ripple signals are aligned vertically so that the cell may be arrayed into a data-path. Historically, bit-slice cells used for arithmetic functions consume less space than standard-height cells.

4. Smartframe and Standard Cell Library

For verification, student projects are submitted to MOSIS for fabrication. To facilitate testing, the students are provided with a Smartframe which consists of a pad-frame AND a built-in self-test (BIST) capability. Student projects can be placed inside the frame and stimulated using patterns generated on-the-fly at full system speed.

The responses are collected and compressed into signatures which are then compared on-chip to hardwired *golden* values obtained from simulation. Thus, the golden values are compared with the live signatures to determine if all is well. If not, raw inputs corresponding to the functional vectors for each student design can be presented to the external pins and the raw outputs observed for debugging purposes. Nearly 100% of the student projects returned using the Smartframe have operated as expected. We attribute this high success rate to this methodology which encourages thorough simulation prior to fabrication.

The Smartframe and a 12-cell standard-height cell library are available at no charge from the University of Tennessee. Composer schematics can be used to interconnect multiple standard cells from this library which can then be automatically placed and routed using Cadence Silicon Ensemble. The resulting layout can also then be viewed using Cadence Virtuoso.

ACKNOWLEDGMENTS

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REFERENCES

- [1] *ECE 651*, University of Tennessee, http://vlsi1.engr.utk.edu/ece/bouldin_courses/
- [2] *MOSIS*, <http://www.mosis.org/>
- [3] *Cadence University Program*, Cadence Design Systems, <http://www.cadence.com/company/university/>
- [4] *Smartframe and Standard-Cell Library*, University of Tennessee, <http://vlsi1.engr.utk.edu/ece/cadence.html>

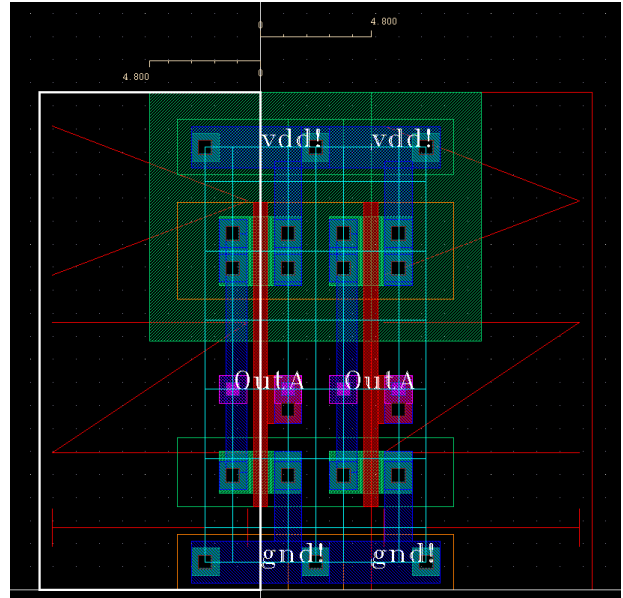


Fig. 2. Overlapping instances of a standard-height cell.

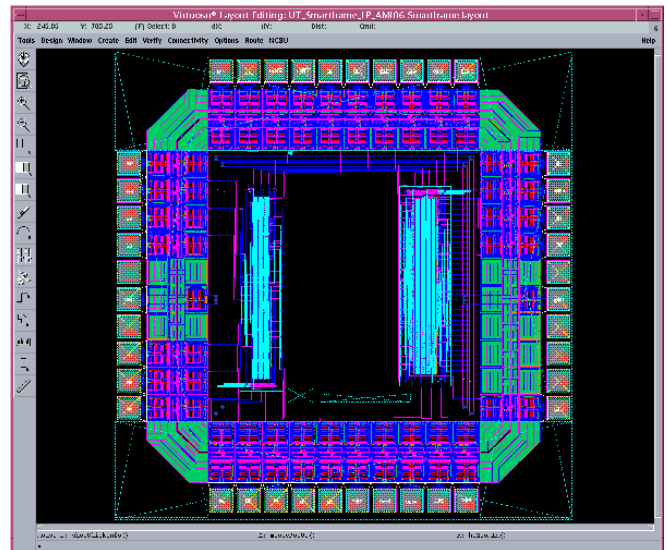


Fig. 3. Smartframe with built-in test for student projects.